

Application No.: 09/655,937  
Amendment dated January 21, 2004  
Reply to non-final Office Action dated October 22, 2003

Docket No.: 8733.289.00

### **REMARKS**

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Non-Final Office Action of October 22, 2003 has been received and its contents carefully reviewed.

In the Non-Final Office Action, the Examiner rejected claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin (U.S. Patent No. 6,323,836); rejected claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. (U.S. Patent No. 6,229,513); and rejected claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3. The rejections of these claims are traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

The rejection of claims 1, 2, 4, 6, 8, 9, 11, 20, and 21 under 35 U.S.C. § 102(e) as being anticipated by Shin is traversed and reconsideration is respectfully requested.

Independent claim 1 is allowable over Shin in that claim 1 recites a combination of elements including, for example, “a timing controller... for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of said line memory to the driving circuit every period of the data clock...” Shin fails to teach, either expressly or inherently, at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 2, 4, and 6, which depend from claim 1, are also allowable over Shin.

Independent claim 8 is allowable over Shin in that claim 8 recites a combination of elements including, for example, “a timing controller... for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the data clock... and for outputting the data in each of the groups to the driving circuit during each period of

the input data clock.” Shin fails to teach, either expressly or inherently, at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claims 9 and 11, which depend from claim 8, are also allowable over Shin.

Independent claim 20 is allowable over Shin in that claim 20 recites a combination of elements including, for example, “a data clock generating step of frequency-dividing an input first data clock at a frequency-division ratio...; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock...” Shin fails to teach, either expressly or inherently, at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 21, which depends from claim 20, is also allowable over Shin.

Further, in rejecting claims 1, 8, and 20, the Examiner cites Shin as teaching “...a timing controller (220), being connected to the line memory (230) and the driving circuit (270), for receiving a data clock inputted from the exterior thereof to output the data from the plurality of groups of the line memory (230) to the driving circuit (270) every period of the data clock... (see column 5, line 18-column 6, line 18).”

However, Applicants respectfully submit that, at column 5, lines 28-32, Shin teaches (with reference to Figure 7) wherein:

“...driving circuit... includes a clock generator 200 having an input terminal for receiving a first clock signal CK1 and an output terminal for outputting a second clock signal CK2; a data controller 210 having an input signal terminal for receiving a data signal D and output terminals for outputting an odd video signal D1, ... an even video signal D2...; a plurality of odd data driver ICs 240 each having a ...data input terminal A1 connected to the odd video signal terminal D1...; and a plurality of even data driver ICs each having a ...data input terminal A2 connected to the odd video signal terminal D2...”

Further, Shin teaches at column 5, line 56 to column 6, line 18 (with reference to Figure 8) that

“...a first clock signal is applied. Then, the clock generator 200 produces the second clock signal CK2, the period of which is twice that of the first clock signal CK1: i.e., the clock speed of the second clock signal CK2 is half that of the first clock signal CK1. According to the first clock signal CK1, the first odd data (video signal)d1 is stored in the odd memory 230a and the first even data (video signal)d2 is stored in the even memory 230b. According to the second clock signal CK2, the first odd data d1 and the first even data d2 are sent to the first odd data driver IC 240 and the first even data driver IC 250, respectively. At that time, the second odd data d3 is stored to the odd memory 230a, and the second even data d4 is stored to the even memory 230b according to the first clock signal CK1. The output of the first pair of data (d1 and d2) and the input of the second pair of data (d3 and d4) are performed at the same time. ...After the line data on the one-page data are latched at all the data driver ICs, all the latched data are sent to the data lines at one time”.

Accordingly, Applicants respectfully submit the teachings of Shin are silent to the aforementioned combination of elements in the presently pending claims.

In the “Response to Arguments” section of the outstanding Office Action, the Examiner apparently summarizes the teachings of Shin, stating that Shin “teach[es] that the timing controller receives a clock signal CK1 from the exterior thereof, and generates a second clock signal CK2, which is outputted from the timing controller” and that “[t]he second clock signal CK2 is generated from the received data clock CK1, and data is output from the plurality of groups of the line memory (230) to the driving circuit every period of the data clock signal CK2 (see figure 8).” The Examiner then states that, in the present invention, “the source sampling clocks SSC1 and SSC2 are generated from data DCLK

received by the timing controller from an exterior thereof” and concludes “[t]herefore, the teachings of [Shin] are very similar to that of the disclosed invention.”

Preliminarily, Applicants respectfully submit that it appears as though the Examiner is supporting the present rejection under 35 U.S.C. § 102(e) because, according to the Examiner, “the teachings of [Shin] are very similar to that of the disclosed invention.” It is respectfully submitted, however, that “similarity” between inventions is not the standard with which anticipation is established. Rather, a claim is anticipated only when each and every element of the claim is described, either expressly or inherently, in a single reference (see, for example, M.P.E.P. § 2131). For at least the reasons set forth above, Applicants respectfully submit Shin fails to anticipate the inventions defined at least in claims 1, 8, and 20.

In further view of the Examiner’s statements reproduced above, Applicants respectfully submit that it appears the Examiner has failed to anticipate the invention as actually defined in claims 1, 8, and 20.

For example, it is respectfully submitted that claims 1 and 8 do not recite any element suggesting that data is outputted every period of a clock signal generated from an externally inputted clock signal, or any analog thereof. To reiterate, claim 1 requires, among other elements, “a timing controller ... receiving a data clock inputted from the exterior thereof to output ...data ...to the driving circuit every period of the data clock...,” and claim 8 requires, among other elements, “a timing controller ...receiving a data clock inputted from the exterior thereof to generate a first data clock ...and ...outputting the data ...to the driving circuit during each period of the input data clock.” As can be seen from the above, the timing controller as claimed in claims 1 and 8 can be reasonably interpreted as outputting data every period of a received, externally inputted data clock. It is respectfully submitted, however,

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that claims 1 and 8 cannot be reasonably interpreted as disclosing a relationship between a clock signal generated in response to a received, externally inputted clock signal and the outputting of data. Claim 20 requires, among other elements, "a data clock generating step of frequency-dividing an input first data clock ...to generate a second data clock; a data outputting step of outputting a desired data unit from each of said groups at a different time during one period of the second data clock..." While claim 20 does recite a relationship clock signal generated in response to a received, inputted clock signal and the outputting of data, claim 20 requires that data from different groups be outputted at different times during a period of the generated clock signal. It is respectfully submitted that Shin is entirely silent with respect to at least this aspect of claim 20. Col 9

The rejection of claims 3, 5, 7, 10, and 12 under 35 U.S.C. § 103(a) as being unpatentable over Shin in view of Nakano et al. is traversed and reconsideration is respectfully requested.

Applicants respectfully submit that claims 3, 5, 7, 10, and 12 are allowable at least because these claims depend from independent claims 1 and 8, which are believed to be allowable.

The rejection of claims 13-19 under 35 U.S.C. § 103(a) as being unpatentable over Nakano et al. in view of the Related Art shown in Figure 3 is traversed and reconsideration is respectfully requested.

Independent claim 13 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 13 recites a combination of elements including, for example, "...a line memory for receiving two pixel data unit sequentially from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data

therein and for outputting the two pixel data unit from each of the groups; ...and a timing controller ...connected to the line memory and the driving circuit, for receiving a data clock inputted from the exterior thereof to generate a first data clock by frequency-dividing the input data clock ...and for outputting the two pixel data ...to the driving circuit during each period of the input data clock.” Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicants respectfully submit that claims 14-17, which depend from claim 13 are also allowable over Nakano et al. in view of the Related Art shown in Figure 3.

Independent claim 18 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 in that claim 18 recites a combination of elements including, for example, “a latch circuit for latching and outputting two pixel unit inputted from the exterior thereof; a driving circuit... connected to the latch circuit...; and a timing controller... connected to the latch circuit and the driving circuit, for receiving a data clock inputted from the exterior thereof to output each one pixel data to the driving circuit at a desired time interval during one period of the data clock.” Neither Nakano et al. nor the Related Art shown in Figure 3, singly or in combination, teach or suggest at least these features of the claimed invention. Accordingly, Applicant respectfully submits that claim 19, which depends from claim 18, is also allowable over Nakano et al. in view of the Related Art shown in Figure 3.

Further, the Examiner cites Nakano et al. as failing to “specifically teach that the memory receives two-pixel unit...” and states Nakano et al. “does... teach that the first and second memories (112, 113) stores display data of an amount corresponding to a total number (2n) of the drain signal lines (D) connected to two drain drivers (130)” and “with reference to a second embodiment, a liquid crystal display of higher resolution has two bus lines (134a, b)

as display data bus lines, and drain drivers (130') are connected thereto (see column 7, lines 43-50).

Column 7, lines 43-50 of Nakano et al. includes the textual passage apparently corresponding to the alleged "second embodiment" of Nakano et al. describing what is illustrated in Figures 5A and 5B of Nakano et al. At column 3, lines 41-45 in the BRIEF DESCRIPTION OF THE DRAWINGS section, Nakano et al. states "FIG. 5A is a block diagram illustrating an exemplary approach, considered by the present inventors and others, for transmitting a display data from the display control unit to drain drivers..." Accordingly, Applicants respectfully submit the disclosure of Nakano et al. directed to Figures 5A and 5B actually disclose what is admitted to be conventional art. At column 7, line 58 – column 8, line 2, Nakano et al. states

"The approach illustrated in FIGS. 5A, 5B, however, requires a twice wider bus width for the display data bus line..., thereby causing an increase in the number of pins required for the display control unit 110, an increase in the number of layers and the area of the printed wiring board, on which the display control unit 110 is mounted. This further leads to an increase cost for the display control unit 110 and the associated printed wiring board, and a larger size of a connector attached to the printed wiring board..."

Accordingly, Applicants respectfully submit the "second embodiment" cited by the Examiner is equivalent to a "prior art embodiment" which teaches away from the actual inventive concept as taught by Nakano et al. at column 4, line 32 through column 7, line 42. Therefore, Applicants respectfully submit the "second embodiment" of Nakano et al. cannot, absent impermissible hindsight reasoning, be combined with the inventive concept of Nakano et al. to arrive at the combination of elements in the present invention.

In the "Response to Arguments" section of the outstanding Office Action, and in response to Applicants' arguments that the Examiner has provided no motivation why one of ordinary skill in the art would be motivated to combine the teachings of the two embodiments and arrive at the claimed invention, the Examiner stated "[Nakano et al.] teaches all that is required by the claim except, that the memory receives two-pixel data unit... but teaches with reference to a different embodiment that the first and second memories (112, 113) stores display data of an amount corresponding to a total number ( $2n$ ) of the drain signal lines (D) connected to two drain drivers (130)." The Examiner then asserts, "[t]herefore" that

"there is a suggestion that it is possible for the memory to receive two pixel data units from the exterior thereof and dividing the data for at least one line into a plurality of groups to store the divided data therein and for outputting the two pixel data unit from each of the groups, since it is possible for the memories to store display data of an amount corresponding to the total number of the drain signal lines, in order to increase the resolution of the driven display..."

Applicants respectfully submit, however, that Nakano et al. teaches, at column 7, lines 3-17 wherein

"...originally ordered display data transmitted from the computer side are inputted to a first memory 112 (or a second memory 113). The first memory 112 (and the second memory 113) stores display data of an amount corresponding to a total number  $2n$  of the drain signal lines D connected to two drain drivers 130 ( $n$  being a positive integer).

In the example illustrated in FIG. 4A, the  $2n$  originally ordered display data transmitted from the computer side are first written, for example, into the first memory 112. When  $2n$  display data are stored in the first memory 112, next  $2n$  display data transmitted from the computer side are written into the second memory 113, and meanwhile the display data are read from the first memory 112 in an order shown in FIG. 4B and outputted to the drain drivers 130 through the display data bus line 134."



Accordingly, Applicants respectfully submit Nakano et al. can be reasonably understood as disclosing, with respect to Figures 4A and 4B, a memory that receives a single exterior pixel data unit which is subsequently divided. However, it is respectfully submitted that Nakano et al. cannot be reasonably interpreted as teaching or even suggesting that the memory 112 and 113 receives two exterior pixel data units, divides the data for at least one line into a plurality of groups, stores the divided data therein, and outputs the two pixel data units from each of the groups during each period of the input data clock as required, at least in part, by claim 13. Similarly, Applicants respectfully submit Nakano et al. fails to teach or suggest a latch circuit for latching and outputting two externally inputted pixel units and a timing controller connected to the latch circuit for receiving an externally inputted clock signal and for outputting each one pixel data to the driving circuit during one period of the data clock as required, at least in part, by claim 18.

Accordingly, it is respectfully submitted that a teaching from Nakano et al. where memories 112 and 113 store data to be outputted to 2n number of drain signal lines does not reasonably suggest the obviousness of at least the aforementioned combination of elements. Absent any such suggestion, Applicants respectfully submit it appears that the Examiner has attempted to arrive at the claimed invention via the impermissible use of hindsight reasoning.

Claim 14 depends from independent claim 13 and, therefore, includes at least the aforementioned combination of elements set forth in claim 13. As described above Nakano et al. fails to teach at least the aforementioned combination of claimed elements. The Related Art shown in Figure 3 was cited as allegedly disclosing the various elements of claim 14. Even if the Related Art shown in Figure 3 actually does disclose the various elements asserted by the Examiner, the Applicant respectfully submits the Related Art shown in Figure

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3 fails to cure the aforementioned deficiencies of Nakano et al. Accordingly, the Applicant respectfully submits that claim 14 is allowable over Nakano et al. in view of the Related Art shown in Figure 3 by virtue of its dependence from claim 13.

Applicants believe the application in condition for allowance and early, favorable action is respectfully solicited. If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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